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Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model

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Design verification is a bottleneck on modern SoC design. Very often, modern SoCs contain both digital blocks and analog blocks. While the metric-driven verification methodology exists for digital verification, analog and mixed-signal design verification relies heavily on SPICE simulation and manual modeling, a process known to be time consuming and error prone. In this talk, we will introduce a new technology that can turn automatically a SPICE netlist into a SystemVerilog model, and thus allows metric-driven digital verification methodologies and tools to be used for analog and mixed-signal design verification. This breakthrough is based on a new theory of signal abstraction developed under a recent DARPA sponsored research program. We will show that how signal-driven abstraction allows various circuit analysis techniques developed in the past several decades including symbolic analysis, Laplace transform, pole/zero extraction and fractional expansion, event-driven analog modeling, interval mathematics, modified nodal analysis, regression, wreal and real number modeling, language compilation, analog assertion, can all be integrated in this unified framework, and to be used in a methodology transparent to designers. Practical examples from 28Gbps SerDes design will be used to illustrate the methodology. In particular, this talk will show the design verification of 28-Gb/s serial transceiver link adaptation and equalization, which were not feasible previously. This research has been supported by the US DARPA IRIS program.

Primary author: Prof. SHI, Richard

Presenter: Prof. SHI, Richard

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