SMACD 2018 & PRIME 2018

Report of Contributions

https://indico.fjfi.cvut.cz/e/103

Contribution ID: **2** Type: **not specified**

Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model

Design verification is a bottleneck on modern SoC design. Very often, modern SoCs contain both digital blocks and analog blocks. While the metric-driven verification methodology exists for digital verification, analog and mixed-signal design verification relies heavily on SPICE simulation and manual modeling, a process known to be time consuming and error prone. In this talk, we will introduce a new technology that can turn automatically a SPICE netlist into a SystemVerilog model, and thus allows metric-driven digital verification methodologies and tools to be used for analog and mixed-signal design verification. This breakthrough is based on a new theory of signal abstraction developed under a recent DARPA sponsored research program. We will show that how signal-driven abstraction allows various circuit analysis techniques developed in the past several decades including symbolic analysis, Laplace transform, pole/zero extraction and fractional expansion, event-driven analog modeling, interval mathematics, modified nodal analysis, regression, wreal and real number modeling, language compilation, analog assertion, can all be integrated in this unified framework, and to be used in a methodology transparent to designers. Practical examples from 28Gbps SerDes design will be used to illustrate the methodology. In particular, this talk will show the design verification of 28-Gb/s serial transceiver link adaptation and equalization, which were not feasible previously. This research has been supported by the US DARPA IRIS program.

Contribution ID: **3** Type: **not specified**

Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model

Thursday, 5 July 2018 09:00 (1 hour)

Design verification is a bottleneck on modern SoC design. Very often, modern SoCs contain both digital blocks and analog blocks. While the metric-driven verification methodology exists for digital verification, analog and mixed-signal design verification relies heavily on SPICE simulation and manual modeling, a process known to be time consuming and error prone. In this talk, we will introduce a new technology that can turn automatically a SPICE netlist into a SystemVerilog model, and thus allows metric-driven digital verification methodologies and tools to be used for analog and mixed-signal design verification. This breakthrough is based on a new theory of signal abstraction developed under a recent DARPA sponsored research program. We will show that how signal-driven abstraction allows various circuit analysis techniques developed in the past several decades including symbolic analysis, Laplace transform, pole/zero extraction and fractional expansion, event-driven analog modeling, interval mathematics, modified nodal analysis, regression, wreal and real number modeling, language compilation, analog assertion, can all be integrated in this unified framework, and to be used in a methodology transparent to designers. Practical examples from 28Gbps SerDes design will be used to illustrate the methodology. In particular, this talk will show the design verification of 28-Gb/s serial transceiver link adaptation and equalization, which were not feasible previously. This research has been supported by the US DARPA IRIS program.

Primary author: Prof. SHI, Richard

Presenter: Prof. SHI, Richard

Session Classification: Plenary Talks

Contribution ID: **4** Type: **not specified**

Challenges in Analog/Mixed-Signal Design Automation

Wednesday, 4 July 2018 09:00 (1 hour)

The traditional view of electronic design automation has intensively focused on the design, synthesis, and layout of digital circuits. This perspective has been reinforced by the trends from Moore's law, which have seen digital system complexities grow exponentially, prompting an acute need for efficient design tools and flows. In contrast, analog design has remained largely focused on the expert designer. This world view is now changing, for several reasons. First, several tasks in analog design are now at a point where they can be realistically automated, notably tasks related to layout automation. In advanced finFET technologies, the reduction in the degrees of freedom due to restricted design rules actually makes layout automation easier. Second, the clear distinction between analog and digital designs has blurred, with modern designs seeing a great deal of digital-like circuitry that assists in implementing analog functionalities. For these structures, established techniques from digital system design can carry over to enable design automation. Third, the complexity of the mixed-signal design space makes it difficult for designers to fully comprehend and compensate for the impact of phenomena such as process variations and device aging. Especially under stringent design specifications, these complexities create openings for design automation tools that can complement the knowledge of the expert designer. Thus, analog and mixed-signal design, which has long been the bastion of the expert designer, is projected to be the new frontier in design automation. This talk will present a brief history of prior efforts and will overview the set of opportunities and challenges in this emerging field.

Primary author: Prof. SAPATNEKAR, Sachin

Presenter: Prof. SAPATNEKAR, Sachin

Session Classification: Plenary Talks

Contribution ID: **5** Type: **not specified**

Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model

Thursday, 5 July 2018 13:00 (1 hour)

Today's image sensor solutions for demanding applications like automotive driver assist image sensing, high speed machine vision, and low power battery operated cameras started from relatively modest solutions for pixels and analog readout design. These initial solution options have evolved along different paths. Now the designer must understand the overall image system requirements to decide where and what to process in the pixel domain, analog circuit domain, and digital processing domain. These decisions rely on understanding the fundamentals of imager photon capture, noise components, analog/digital signal processing topology efficiency, and now the impact of 3D wafer stacking on sensor architecture solutions. This talk will review some of the fundamentals of image sensor technology, design, how it evolved to its current state, and the trajectory for what is possibly next.

Primary author: Mr PANICACCI, Roger

Presenter: Mr PANICACCI, Roger

Session Classification: Plenary Talks