SMACD 2018 & PRIME 2018

Tuesday, 3 July 2018

Plenary Talks: Marcel Urban (AMS) - Room 103 (09:00 - 10:00)

Wednesday, 4 July 2018

Plenary Talks: Sachin Sapatnekar (U. Minnesota) - Room 103 (09:00 - 10:00)

time	[id] title	presenter
09:00	[4] Challenges in Analog/Mixed-Signal Design Automation	Prof. SAPATNEKAR, Sachin

Thursday, 5 July 2018

Plenary Talks: Richard Shi (U. Washington) - Room 103 (09:00 - 10:00)

time	[id] title	presenter
09:00	[3] Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model	Prof. SHI, Richard

Plenary Talks: Roger Panigacci (On Semiconductors) - Room 103 (13:00 - 14:00)

time	[id] title	presenter
13:00	[5] Accelerating Mixed-Signal Design Verification: Turn a SPICE netlist into a SystemVerilog Model	Mr PANICACCI, Roger