My ITS3 work at CERN

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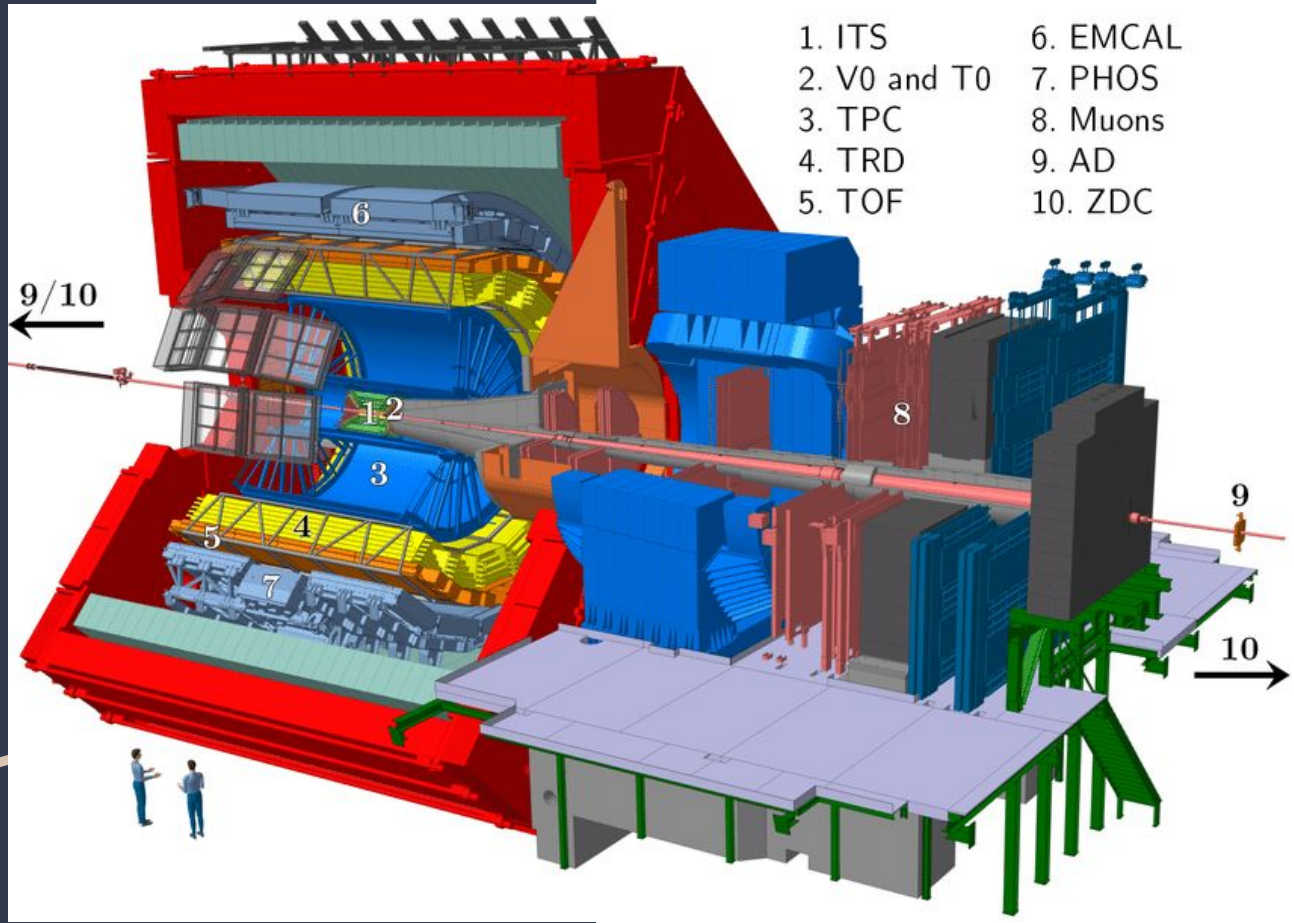
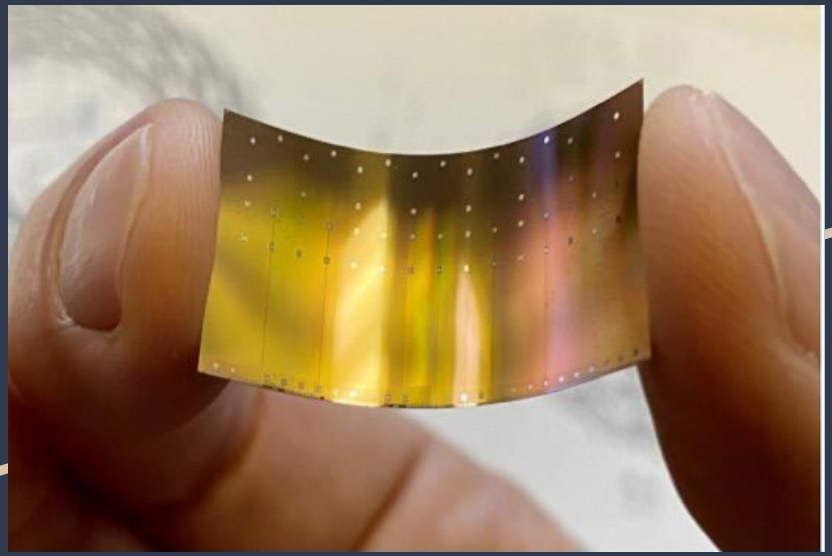
with Hartmut Hillemanns and Nicola Minafra
20/09/2023

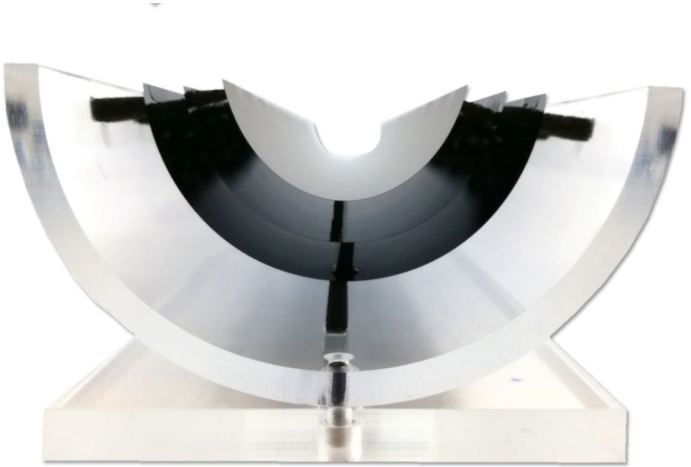
ITS


1. ITS
2. V0 and T0
3. TPC
4. TRD
5. TOF
6. EMCAL
7. PHOS
8. Muons
9. AD
10. ZDC
9/10
6
1
2
3
4
5
7
8
9
10

ITS3

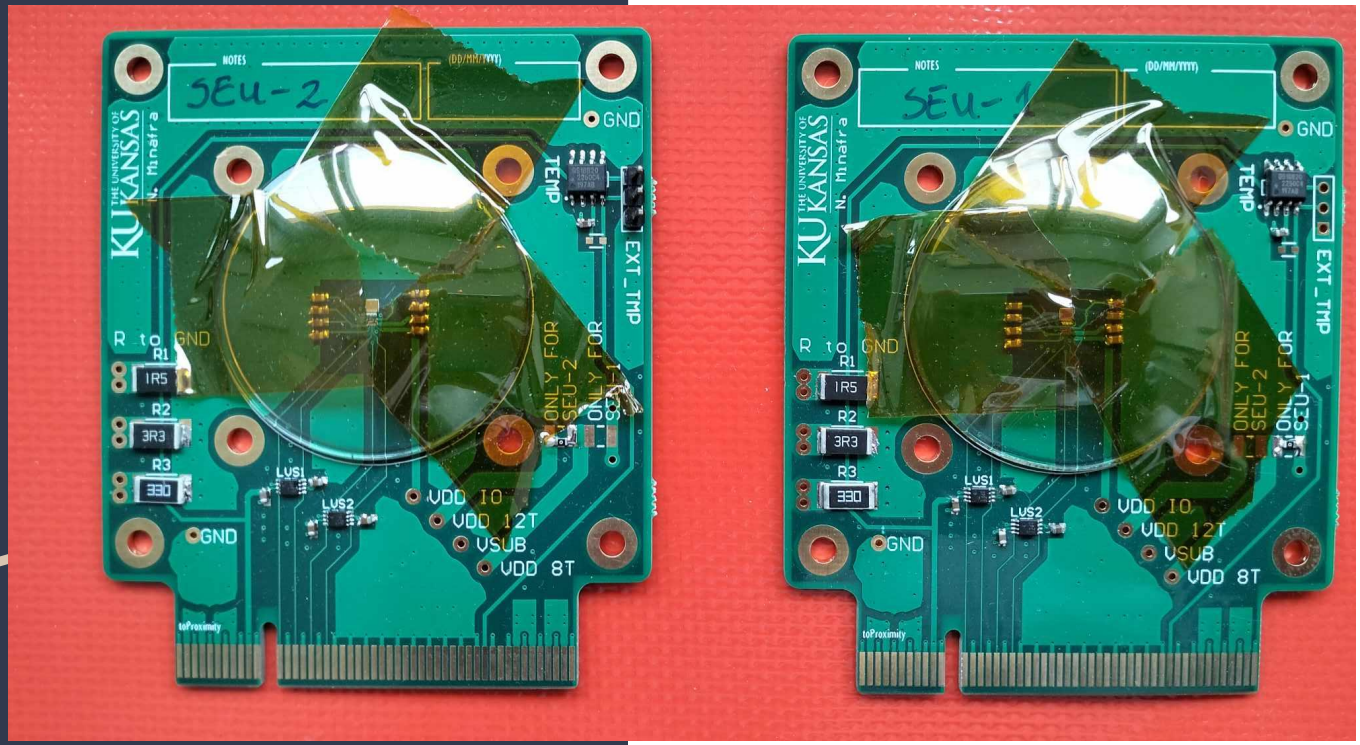


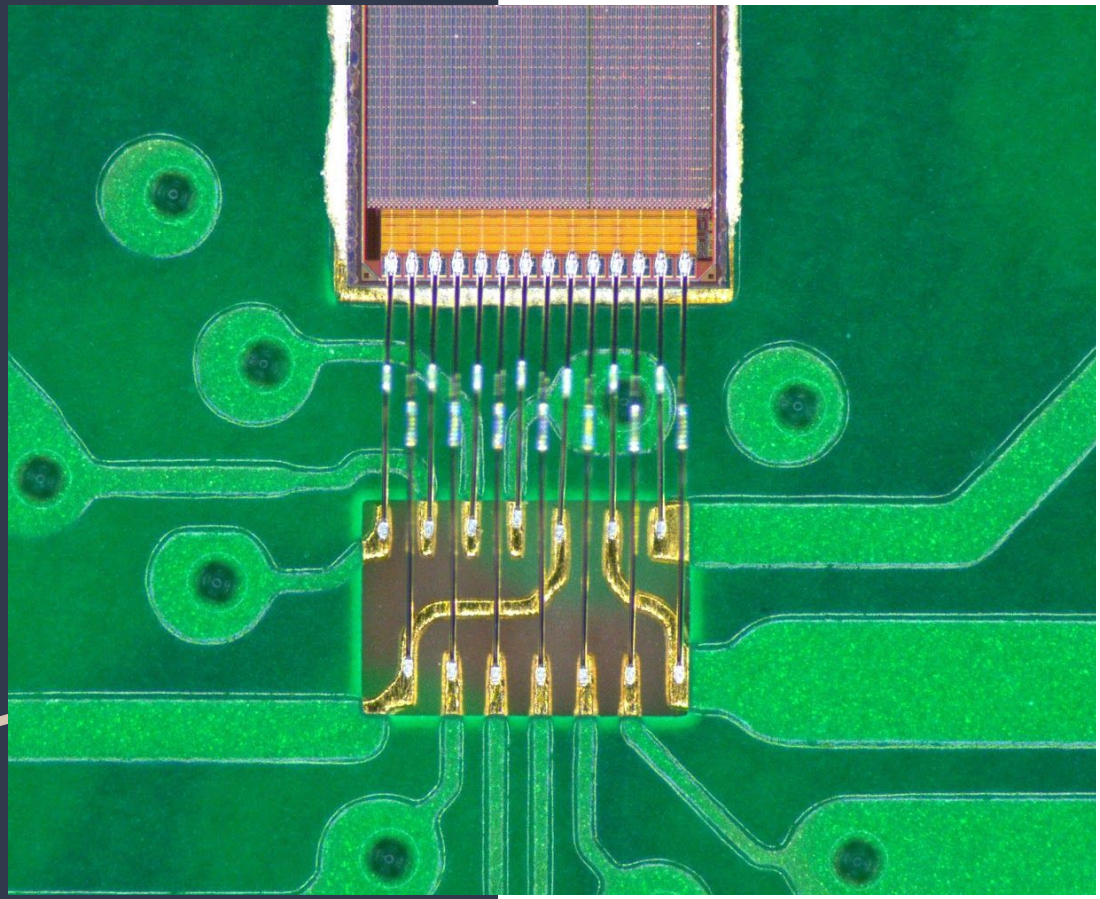
- closer to the beam
- smaller pipe
- lower material budget



SEU memory chips

- ring buffer and RAM



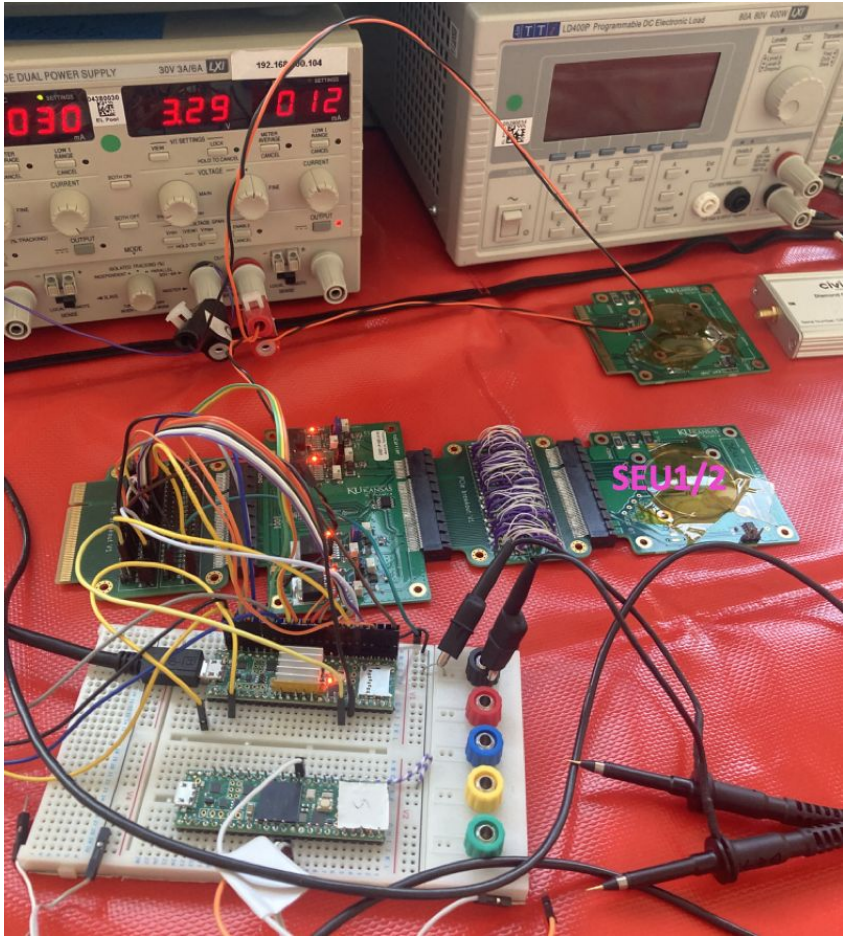


Problems

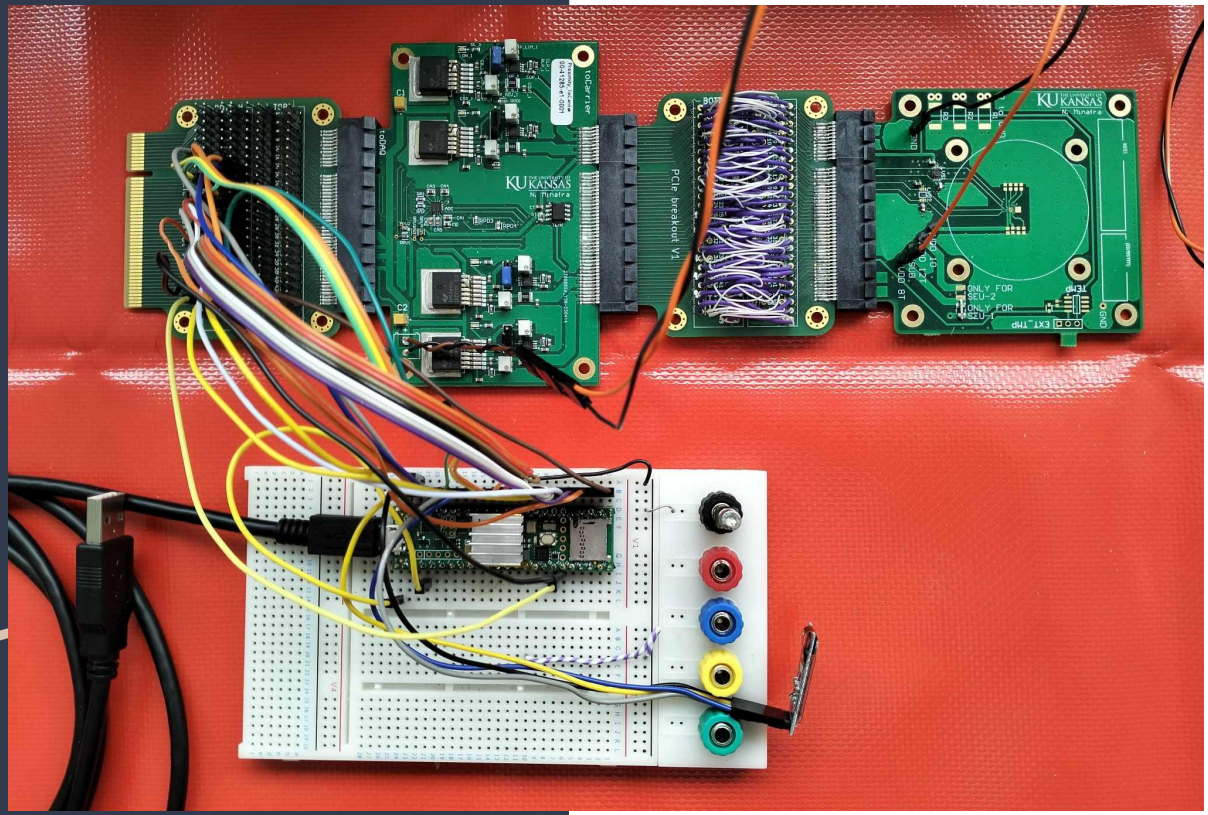
- latch-up
  - short circuit caused by deposited energy of ionising particle

- single event upset
  - change of state (bit flip) caused by single ionising particle

Setup with an emulator

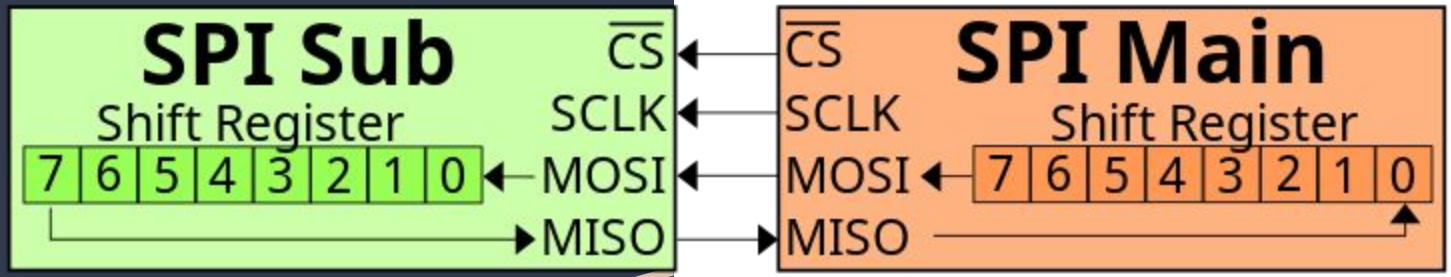


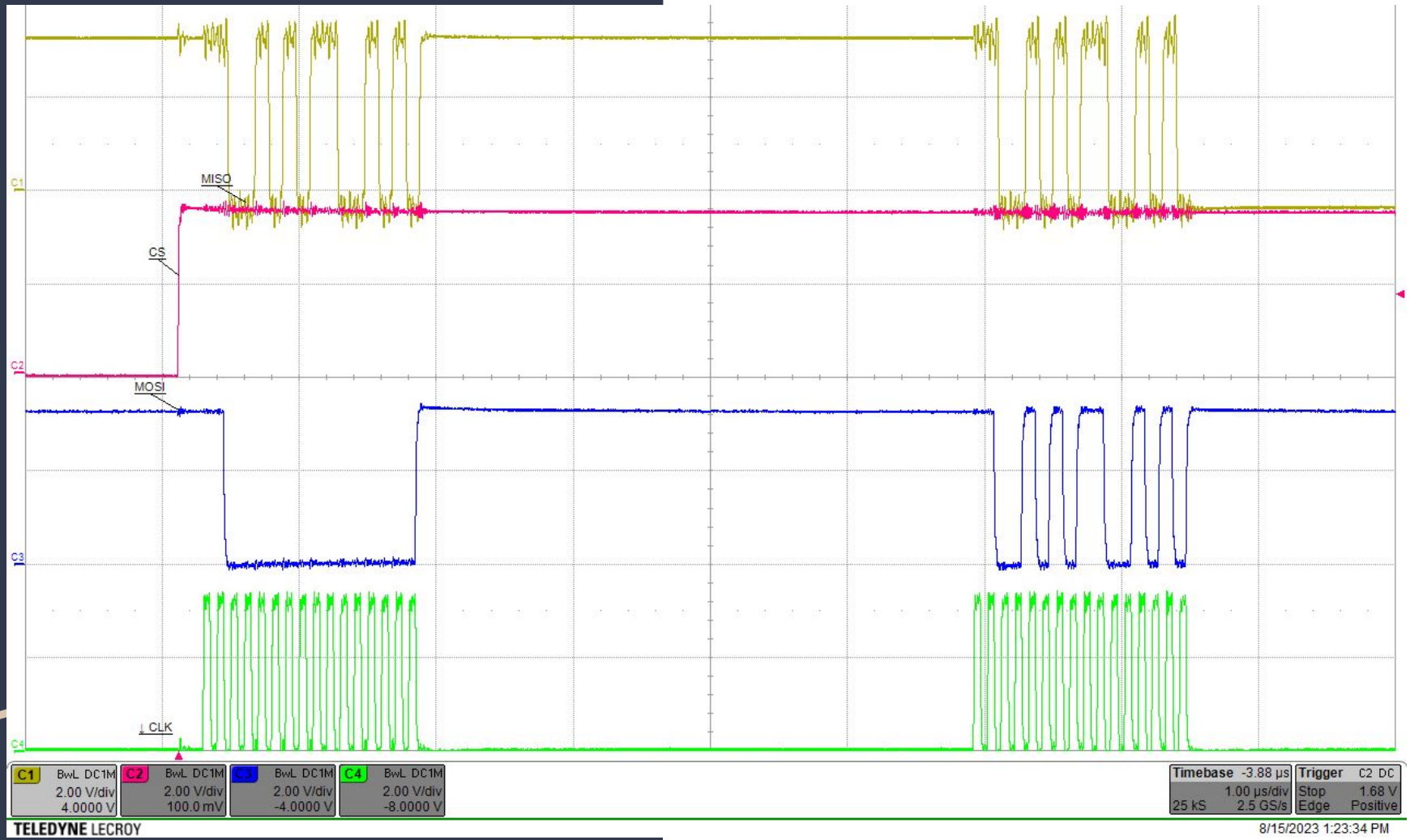
Setup

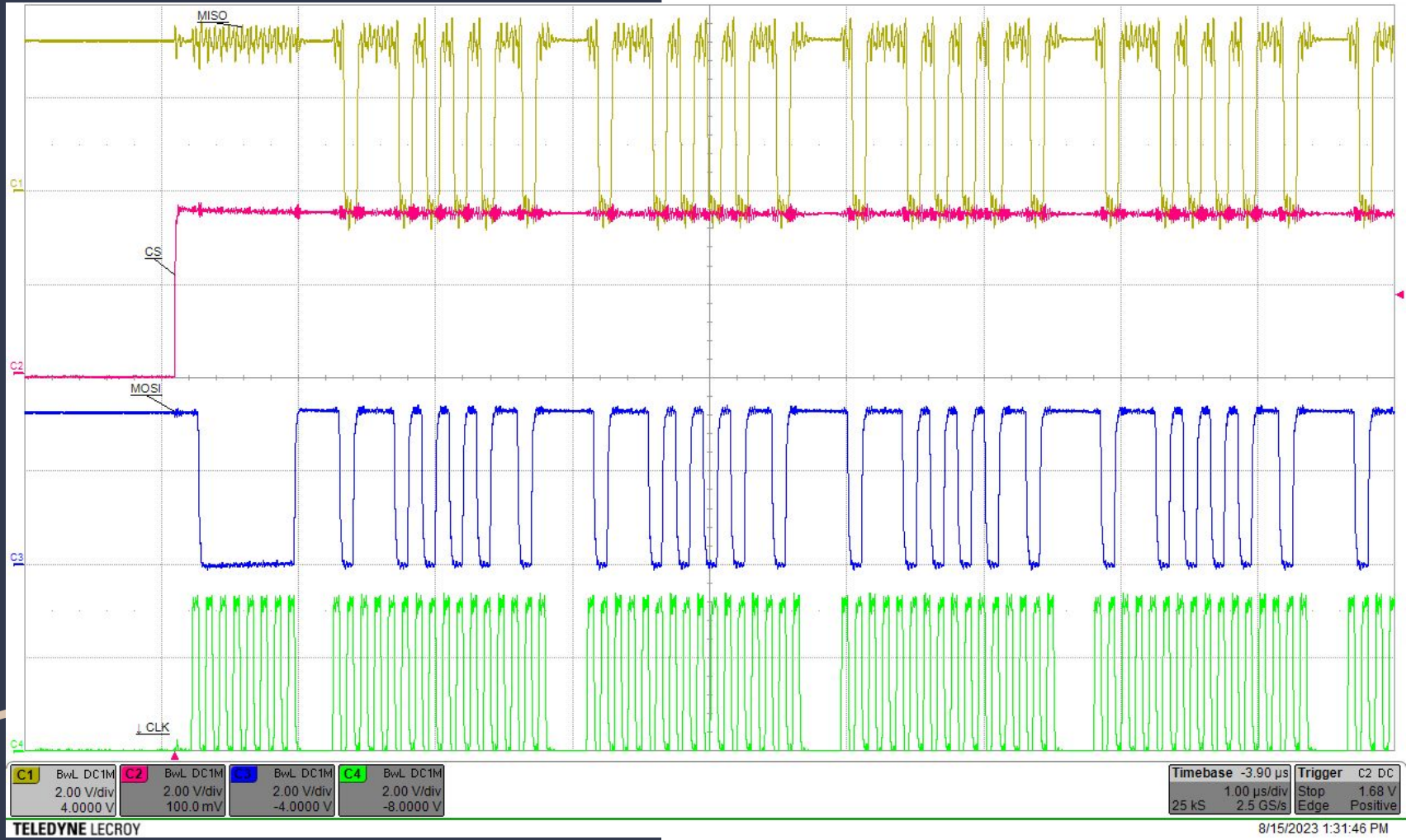

PCIe breakout V1
KU KANSAS
ONLY FOR SEU-2
ONLY FOR SEU
EXT_TMP
TEMP
GND

SPI

- chip select
- serial clock
- main out sub in
- main in sub out




MISO
CS
MOSI
CLK
C1
C2
C3
C4
C1 BwL DC1M 2.00 V/div 4.0000 V
C2 BwL DC1M 2.00 V/div 100.0 mV
C3 BwL DC1M 2.00 V/div -4.0000 V
C4 BwL DC1M 2.00 V/div -8.0000 V
Timebase -3.88 µs 1.00 µs/div 25 kS 2.5 GS/s
Trigger C2 DC Stop 1.68 V Edge Positive
TELEDYNE LECROY
8/15/2023 1:23:34 PM


MISO
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C2 BwL DC1M 2.00 V/div 100.0 mV
C3 BwL DC1M 2.00 V/div -4.0000 V
C4 BwL DC1M 2.00 V/div -8.0000 V
Timebase -3.90 µs 1.00 µs/div 25 kS 2.5 GS/s
Trigger C2 DC Stop 1.68 V Edge Positive
TELEDYNE LECROY
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Summary of my work

- development of the firmware for the Teensy DAQ
- development of the firmware for the SPI sub emulator
- development of the test algorithms
- development of the python control code
- test and debug of the code
- test of the wire-bonded chips

Next steps

- irradiation tests in Leuven and Prague :)